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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,308	05/15/2001	Zahid Najam	10736/9	3090

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,308	NAJAM ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1,2,5,11,12,15,23-26,28,,34,36,42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ali et al. (Patent No. 6,289,421)in view of Greim et al.(patent No. 6,678,801).

2. Ali taught (as per claims 1,11,34) the invention substantially as claimed including a data processing ("DP") system comprising:

a) a processor (20) (e.g., see figs. 1.2);

b) A co-processor (10) separated from the processor by a boundary(e.g., see figs. 1,2);

c) An interface (1) coupled with the processor (20) and said co-processor(10), comprising memory (first buffer 6,7) having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other at least two ports operative to bridge the boundary(e.g., see figs. 1,2,3 and col. 4, line 8-col. 5, line 31);

d) Control logic coupled with said at least two read/write ports (e.g., see col. 4, line 58-col. 5, line 52);

e) wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory (e.g., see col. 3, line 32-col. 4, line 7 and col. 4, lines 47-65);

f) said coprocessor stores data intended for said processor to said memory and reads data stored by said co-processor from said memory independent of said co-

processor said co-processor stores data intended for said processor to said memory and reads data stored from said memory (e.g., see col. 4, lines 47-65); and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; and wherein said processor and said coprocessor are capable of storing data to said memory substantially simultaneously (e.g., see col. 4, line 57-col. 5,line 52 and col. 2, lines 20-34).

3. Ali did not expressly detail the control logic detecting when the coprocessor has stored data and to signal the processor or detecting when the processor has stored data to the memory and signaling the coprocessor (claims 1,11, 24, 34). Greim however taught control logic detecting data stored in a interface with a dual port memory(that acts as a message buffer) by an source processor and sending an interrupt to the destination processor (e.g., see col. 25, lines 10-col. 26, line 32 and col. 23, line 16-col. 24, line 67)[the logic determines if a mailbox is written to and determines if a destination mailbox bit is enabled for determining when to send an interrupt to the destination processor]. Greim also taught the interrupt sent to the destination indicated data was stored and needed to be read by the destination and the destination could read all the contents(e.g., see col. 37, lines 17-51).

4. Greim did not expressly detail (claim 24,25) receiving a read command from the coprocessor or processor. However, in the Greim teachings the destination processor received an interrupt indicating data was stored in the interface and needed to be read by the destination processor and could be serviced by reading the data in the mailbox by the destination. Therefore since the Greim system sent interrupt to plural processors

for stored messages then one of ordinary skill would have been motivated to have the particular destination processor of the plurality of processors send a read command when it was ready to read the data in the message buffer at least to provide proper control of sending the data to be read such as was well known in the art with respect to handshaking signals for access of data between systems. Note the in with the combination of the Ali and Greim teachings at least one destination processor would have been a coprocessor when the processor sent a message and the destination would have been the processor when the coprocessor sent a message.

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Ali and Greim. Both references were directed to the problems for transferring data between processors using dual port memory. One of ordinary skill would have been motivated to incorporate the Greim teachings of interrupting the destination processor using the dual port memory interface at least to release the source processor from any tasks in the ensuring that the data reaches its destination and therefore reducing the load on the processors in the combined system.

6. As to the limitations of claim 2,12,23,26 Ali taught the processors on different cards or boards and therefore the boundary would have comprised a printed circuit board to printed circuit board connected couple to the processor and co-processor (e.g., see figs 1, 2,3). The use of connectors that isolate the connected devices from the bus were well known in the art at the claimed invention. One of ordinary skill implementing the Ali and Greim system would have been motivated to use these tristate type connectors to at least protect the connected devices for electrical surges when not

actively transferring data and to reduce power drain a from plural elements and connected to the bus and ensure stability of signals transferred bus without interference.

7. As to claim 5,15,28,36 Ali taught the co-processor comprising a task specific processor (DSP) (e.g., figs, 1,2 and col. 3, line 32-53).

8. As per claims 42-45. Greim taught the memory interface logic detecting that the data stored was for a particular processor by checking status information stored by the destination processor (e.g., see col. 25, lines 1-62).

9. Claims 3,4,6,7,8,9,10,13,14,16,17, 18,19,20,21,22, 27,29,30,31,32, 33,35, 37, 38,39,40,41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ali and Greim as applied to claims 1,2,5,11,24,34, above, and further in view of Kowalczyk (patent No. 4,744,078)(cited in the last office action).

10. As per claim 3,4,13,14,27,35 Kowalczyk taught transfer between a system bus and a network bus. Therefore one of ordinary skill have been motivate to connect the best available network devices to the network bus. Since at least some network devices would have comprised different characteristics for the transferred data such as word length or encoding etc.(especially when they were from different manufacturers) then in at least one implementation of the Ali and Greim and Kowalczyk teachings the boundary would have comprised different protocols. Clearly the processor connected to the network bus would have comprised an network processor.

11. As per claim 6,7,16,17,29,30,37,38 One of ordinary skill would have been motivated to connected off the shelf components to aid the processor in processing

data. Since the Kowakczyk taught a network bus one of ordinary skill would have been motivated to connected the system to various type of networks including the INTERNET. In applications that would be characteristic of searching volumes of data via the INTERNET one of ordinary skill would have been motivated to coupled a classification coprocessor and an content addressable memory to search for data especially when the co-processor is used a conventional search engine.

12. As per claims 8,9,18,19,31,39 Kowalczyk taught control logic signals via the connected buses when data is stored in the data memory (e.g., see col. 4, lines 1-31). Considering the devices connect to the buses would have comprised processor and co-processors (especially considering teachings of Ali and Greim) the signals to the bus would have been transmitted to the processor and co-processor.

13. As per claim 10,20,32,40 Kowalczyk taught the memory comprises a dual ported synchronizing random access memory (10). Since Kowalczyk did not detail refresh of the memory it would have been obvious to one of ordinary skill that the memory would have comprised a static random access memory. As to the burst capability of the memory since the memory is allowing switching of transfer between two buses one of ordinary skill would have been motivated to select an off the shelf memory with burst capability to facilitate quick transfer when a lot of data was being transferred.

14. As per claims 21,22,33,41 The control logic of Kowalczyk performs that task for determining when to transfer data as described above and therefore allows the processor to communicate with the coprocessor as if the co-processor was directly connected with the processor. Also Since the Kowalczyk interface establishes the

network protocol (e.g., see col. 2, lines 41-57) The interface allows the processor to operate independently of the interface requirements of the coprocessor (that would have been connected to the network bus).

15. It would have been obvious to one of ordinary skill to combine the teachings of Ali and Kowalczyk. Both references were directed toward control of transfer of data between system devices via a memory with plural input and outputs. Ali taught the devices for transferring the data were processor and coprocessor that were on different cards or boards. In at least one implementation the transfer of data between the processor memory and coprocessor the processor would have coupled to a system bus. Kowalczyk taught the transfer was between a system bus and a network bus. Clearly the devices in a processing system storing data into a memory for transfer to another device on another bus would have comprised processors. The addition of the control of transfer to be between system bus and network bus would have allowed the combined system to transfer data between processors in a system to co-processors that were connected in a network. This control would have relieved the processor from having to determine when the coprocessor was ready for transfer of data.

Response to Arguments

Applicant's arguments with respect to claims 1-45 have been considered but are moot in view of the new ground(s) of rejection.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Simmons (patent No. 5,406,472) disclosed a multi-lane controller (e.g., see abstract).

Johnson (patent No. 6,622,185) disclosed a system for providing a real-time programmable interface to a genera purpose non-real-time computing system (e.g., see abstract).

Olgiati (patent No. 6,782,445) disclosed a system comprising a processor an coprocessor (e.g., see abstract).

Shakkarawar (patent No. 5,822,768) disclosed a dual ported memory for a unified memory architecture (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER